In the Claims

Please cancel Claims 12, 15 and 16.

Please amend Claims 1-3, 5-7, 9, and 13.

Listing of the Claims

1. (Currently Amended) A method of making a hermetically sealed, wafer level chip scale package, comprising the steps of:

(A) providing a cap for protectively covering active areas on a chip;

(B) applying a layer of metalization on an entire face of the cap;

©)(C) forming a continuous bead of solder completely surrounding said active areas on said chip and contacting said metalization layer;

(D) removing said metalization layer not covered by said continuous bead of solder and assembling the cap and the chip with the solder bead positioned between and contacting the metalization layer and the area on the chip surrounding the active chip areas; and,

(E) melting the solder bead to form a continuous, hermetic seal around the active chip areas between the cap and the chip.

2. (Currently Amended) The method of Claim 1, wherein step ©(C) includes forming the solder bead on the face of the cap having the layer of metalization.

3. (Currently Amended) The method of Claim 2, wherein step (C©) includes:

applying a pattern mask over the metalization layer,

applying a layer of solder through the mask onto the metalization layer.

4. (original) The method of Claim 3, wherein applying the pattern mask includes depositing a layer of photoresist over the metalization layer, exposing and developing the photoresist, and

stripping exposed areas of the photoresist to achieve a desired mask pattern.

5. (Currently Amended) The method of Claim 1, wherein step (C)~~(C)~~ includes an electroplating process step.

6. (Currently Amended) The method of Claim 1, wherein step ~~(C)~~(C) includes:

forming a photoresist pattern mask over the metalization layer,

electroplating a layer of solder material through the mask onto the metalization layer, and

striping away the photoresist pattern mask.

7. (Currently Amended) The method of Claim 6, wherein step (C)~~(C)~~ includes reflowing the solder layer to form the solder bead.

8. (Original) The method of Claim 7, including the steps of:

bonding a spacer onto the cap, and

after step (E) is performed, cutting away a portion of the cap that includes the spacer.

9. (Currently Amended) The method of Claim 1, including the step of forming a spacer on the cap, and wherein:

step ~~(C)~~(C)) is performed by electroplating a layer of solder through a pattern mask onto the metalization layer,

step (D) includes bringing the spacer into face-to-face contact with chip, and

after step (E) is performed, cutting away a portion of the cap to which the spacer is bonded.

10. - 12. (Cancelled)

13. (Currently Amended) A ~~The~~ method of ~~Claim 12~~ making a hermetically sealed, wafer level chip scale package, comprising the steps of:

(A) providing a semiconductor wafer having a plurality of chip portions formed therein, said wafer having a first face and a second opposite face,

(B) providing a cap for protectively covering active areas on each of the chip portions;

(C) applying a layer of metalization on one face of the cap;

(D) applying a plurality of continuous, patterned beads of solder to the metalization layer; applying a plurality of spacers on the cap to maintain a desired spacing between the cap and the wafer;

(E) bringing the cap into face-to-face contact with the wafer such that each of the continuous solder beads contacts and surrounds an active area of a corresponding chip portion;

(F) melting the solder to bond the cap to each of the chip portions and thereby form

a hermetic seal around the active areas of each of the chip portions; and,

cutting the wafer into individual die.

14. (Original) The method of Claim 13, wherein step (G) includes cutting away portions of the cap having the spacers applied thereto.

15 - 25. (Cancelled)